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DICKSTEIN SHAPIRO LLP
1177 AVENUE OF THE AMERICAS 6TH AVENUE
NEW YORK, NY 10036-2714

EXAMINER	
JOHNSON, BRIAN P	

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ROBERT E. OBER, ROGER D. ARNOLD,
DANIEL F. MARTIN, and ERIK K. NORDEN

Appeal 2008-1900
Application 10/712,473[1]
Technology Center 2100

Decided: December 11, 2008

Before: ALLEN R. MACDONALD, JAY P. LUCAS and
THU A. DANG, *Administrative Patent Judges*.

LUCAS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE

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[1] Application filed November 12, 2003. The real party in interest is Infineon Technologies, A.G.

Appellants appeal from a final rejection of claims 1 to 22 and 25 to 36 under authority of 35 U.S.C. § 134. Claims 23 and 24 are canceled. The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

Appellants' invention relates to a method of handling interrupts in a multi-threaded processor to avoid executing lower priority threads before executing higher priority threads (called "priority inversion"). In the words of the Appellants:

> Accordingly, a real-time embedded system in accordance with the invention includes threshold interrupt logic and/or trap-tagging logic for preventing priority inversion, ensuring proper servicing of traps, and preventing unintended trap reentrancy during multi-threaded operation. Interrupt handling logic in accordance with an embodiment of the invention assigns interrupts individual interrupt priority values, while associating a single interrupt threshold value with all active threads. An interrupt must have an interrupt priority value higher than the current interrupt threshold value to be serviced. Therefore, the conditions for priority inversion are eliminated, as any interrupt being serviced will have a higher priority than any pending thread. By adjusting the interrupt threshold value, the system can increase or decrease the number of interrupts that can be accepted by the system.
> (Spec., p. 5)

Claim 1 is exemplary:

1. A method for operating a multi-threaded system having a plurality of active threads, the method comprising:

assigning an interrupt priority value to each of a plurality of interrupts;

specifying an interrupt threshold value; and

processing a requested interrupt only when the interrupt priority value of the requested interrupt is higher than the interrupt threshold value.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Hobbs	US 5,197,138	Mar. 23, 1993
Radhakrishna	US 6,823,414 B2	Nov. 23, 2004

REJECTIONS

R1: Claims 1 to 5, 9 to 16, 20 to 22, 25, 26, 29 to 32, and 34 to 35 stand rejected under 35 U.S.C. § 102(b) for being anticipated by Hobbs.

R2: Claims 6 to 8, 17 to 19, 27 to 28, 33, and 36 stand rejected under 35 U.S.C. 103(a) for being obvious over Hobbs in view of Radhakrishna.

Appellants contend that the claimed subject matter is not anticipated by Hobbs, or rendered obvious by Hobbs in combination with Radhakrishna, for failure of Hobbs to teach a critical claimed limitation. The Examiner contends that each of the claims is properly rejected.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Briefs and the Answer for their respective details. Only those arguments actually made by Appellants have been considered in this opinion. Arguments which Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived.

We affirm the rejection.

ISSUE

The issue is whether Appellants have shown that the Examiner erred in rejecting the claims of R1 and R2 under 35 U.S.C. § 102 and 35 U.S.C.

§ 103 respectively. The issue turns on whether the reference Hobbs teaches the claimed limitation of specifying an interrupt threshold value, and processing interrupts only when the interrupts have a priority value higher than the threshold value.

FINDINGS OF FACTS

The record supports the following findings of facts (FF) by a preponderance of the evidence.

1. Appellants have invented a system and method (hereinafter "method") for handling interrupts in multi-thread computer processors. (Spec., ¶ [1].) Appellants' invention relates to avoiding a condition called "priority inversion" in multi-thread processors, where, because of the processing of an interrupt received while processing a lower priority thread, a higher priority thread fails to be processed when it should be. (Fig. 1, ¶ [5], ¶ [6]). Appellants avoid this priority inversion by specifying an interrupt threshold value, and only processing an interrupt if the priority value of the interrupt is higher than the threshold value. (Spec., ¶ [25]). The threshold value is set higher than the priority values of the active threads, so priority inversion is prevented. (Id.).

2. The reference Hobbs teaches a multi-threaded processor in a computer system. (Col. 1, l. 60). Priorities are assigned to the threads being processed by the computer, and to all interrupts seeking to be processed. (Col. 2, l. 53). Hobbs further teaches, "An interrupt will not be recognized or serviced by the processor until the priority of the code thread is lower than the priority of the interrupt." (Col. 2. l. 54-57).

PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375-76 (Fed. Cir. 2005) (citation omitted).

"Anticipation of a patent claim requires a finding that the claim at issue 'reads on' a prior art reference." *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999)

The analysis begins with an interpretation of the claims: "Both anticipation under § 102 and obviousness under § 103 are two-step inquiries. The first step in both analyses is a proper construction of the claims . . . . The second step in the analyses requires a comparison of the properly construed claim to the prior art." *Medichem S.A. v. Rolabo S.L.*, 353 F.3d 928, 933 (Fed. Cir. 2003) (internal citations omitted).

"Though understanding the claim language may be aided by explanations contained in the written description, it is important not to import into a claim limitations that are not part of the claim. For example, a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment." *Superguide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004).

ANALYSIS

From our review of the administrative record, we find that the Examiner has presented a prima facie case for the rejections of Appellants' claims under 35 U.S.C. §§ 102, and 103. The prima facie case is presented

on pages 3 to 11 of the Examiner's Answer. In opposition, Appellants present a number arguments.

Arguments with respect to the rejection of claims 1 to 22 and 25 to 36 under 35 U.S.C. § 102 [R1]and under 35 U.S.C. § 103 [R2]

As the same issue forms the basis for Appellants' argument against rejections [R1] and [R2], the two rejections will be considered together.

Appellants contend that the Examiner erred in rejecting claims 1 to 22 and 25 to 36 because "Hobbs compares the priorities of two different processor functions (i.e., code thread and interrupt), wherein each of these priorities varies. This is different from determining whether a priority of an interrupt is higher than a fixed threshold value, as claimed." (Br., p. 5, middle). The Examiner, on the other hand, points out that "a fixed interrupt value is not claimed." (Ans., p. 16, middle).

The Examiner is correct. A fair reading of Hobbs demonstrates:

- Hobbs assigns an interrupt priority value to each of a plurality of interrupts; (Col. 2, l. 50-52)
- Hobbs specifies an interrupt threshold value, namely that of the priority of the code thread currently being processed; (Col. 2, l. 53-54); and
- Hobbs processes a requested interrupt only when the priority of that interrupt is higher than the specified interrupt threshold value. (Col. 2, l. 54-57).

As the Examiner observed, nothing in the claims requires that the specified interrupt threshold value be fixed or absolute, and we decline to read descriptions from the Specification into the claims. (See *Superguide Corp. v. DirecTV Enterprises, Inc.* cited above.) As all claimed limitations have been met by the references as expressed in the rejections, we decline to find error.

We defer to the Examiner's Answer for an application of this conclusion to the other dependent and independent claims.

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that the Examiner did not err in rejecting claims 1 to 22 and 25 to 36 under 35 U.S.C. § 102 [R1] and 35 U.S.C. § 103 [R2].

DECISION

The Examiner's rejection of claims 1 to 5, 9 to 16, 20 to 22, 25, 26, 29 to 32, and 34 to 35 under 35 U.S.C. § 102(b) for being anticipated by Hobbs is Affirmed.

The Examiner's rejection of claims 6 to 8, 17 to 19, 27 to 28, 33, and 36 under 35 U.S.C. 103(a) for being obvious over Hobbs in view of Radhakrishna is Affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

pgc

DICKSTEIN SHAPIRO LLP
1177 AVENUE OF THE AMERICAS 6TH AVENUE
NEW YORK NY 10036-2714